DATA SHEET

SA1630
IF quadrature transceiver

Product specification

IC17 Data Handbook

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Philips
Semiconductors

PHILIPS

IF quadrature transceiver SA1630

DESCRIPTION

The SA1630 is a 70–400 MHz I/Q transceiver for wireless LAN. The Receive Path contains a digitally gain controlled linear IF amplifier, a pair of quadrature down conversion mixers and a pair of baseband amplifiers. The transmit path contains a pair of quadrature up conversion mixers that transposes a quadrature baseband input signal up to IF frequency. An external VCO signal is divided internally and provides quadrature local oscillator signals for the mixers. Another divider chain, reference divider and phase detector are provided to avoid the need for an external synthesizer. To keep power consumption to a minimum the transmit, receive and local oscillator functions can be powered down under digital control.

FEATURES

- Low supply voltage operation of 2.7V for main chip and 2.9V for charge pump.
- Low current consumption: 33.5 mA in RX, 26.5 mA in TX, typical at 3V.
- Flexible power up/down options.
- Optional 2.5V regulated reference voltage available during transmit.
- Input IF frequency range of 70–400 MHz.
- Internal IF PLL for synthesizing the local IF oscillator signal.
- Bandwidth of baseband Tx inputs is 20 MHz and that of baseband Rx outputs is 8.5MHz.
- Designed for IEEE 802.11 wireless LAN using Direct Sequence Spread Spectrum modulation.
- Control registers power up in a default state.
- Only a standard reference input frequency required, choice of 8, 11, 22 or 44 MHz.
- Digital gain control of 70 dB in steps of 2 dB.
- Rx Baseband amplifiers are capable of driving 1kΩ ||15pF
- Rx Baseband o/p's clamp symmetrically, above 1Vp–p in order to prevent dc bias shift under overdrive conditions.
- Package: LQFP–48, PCMCIA compatible

APPLICATIONS

- IF circuitry for IEEE 802.11 DSSS wireless LAN.
- Applications for high speed wireless data.

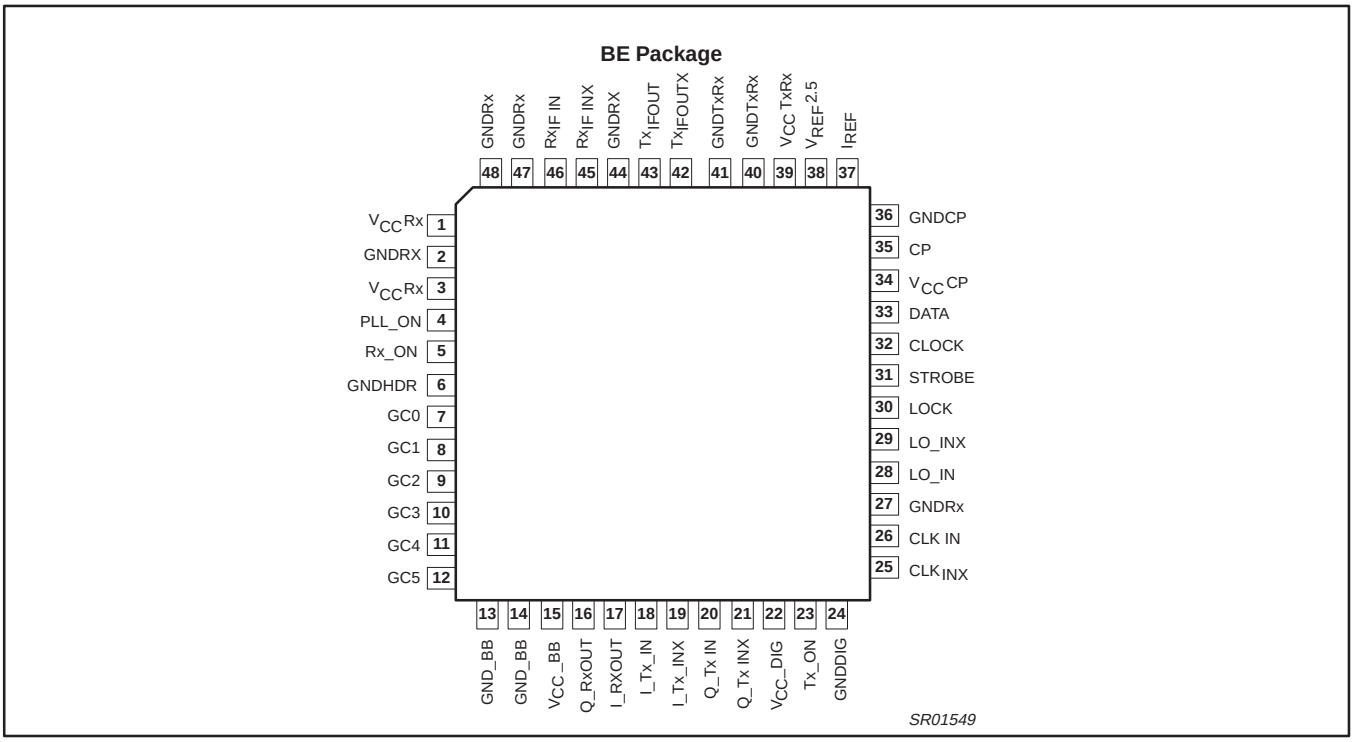


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48–Pin Plastic Low Profile Quad Flat package	–40 to +85°C	SA1630BE	SOT313–2

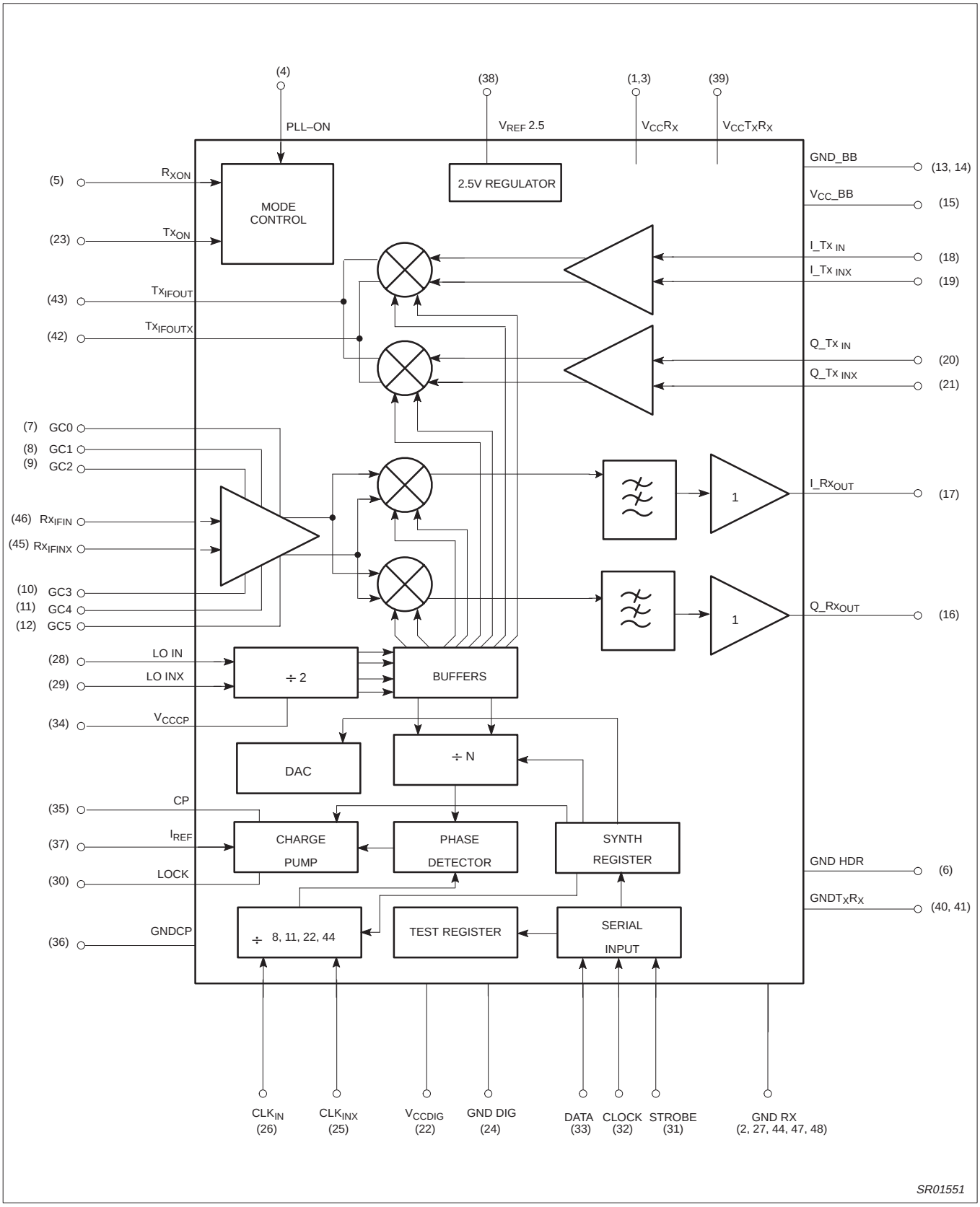


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1, 3	V_{CC}Rx	Supply Pin for Rx section (IF circuits)
2, 27, 44,47, 48	GNDRx	Ground pins for Rx section (IF circuits)
4	PLL_ON	One of the three digital CMOS logic control inputs to the mode control section
5	Rx_ON	One of the three digital CMOS logic control inputs to the mode control section
6	GNDHDR	Substrate ground
7	GCO	Control bit 0 for IF VGA gain control, CMOS input
8	GC1	Control bit 1 for IF VGA gain control, CMOS input
9	GC2	Control bit 2 for IF VGA gain control, CMOS input
10	GC3	Control bit 3 for IF VGA gain control, CMOS input
11	GC4	Control bit 4 for IF VGA gain control, CMOS input
12	GC5	Control bit 5 for IF VGA gain control, CMOS input
13, 14	GND_BB	Ground pin for Rx baseband circuits
15	V_{CC}_BB	Supply Pin for Rx Baseband circuits
16	Q_RXOUT	Quadrature–phase Rx baseband output, single–ended
17	I_RxOUT	In–phase Rx baseband output, single–ended
18	I_Tx IN	In–phase differential Tx baseband input, positive
19	I_Tx INX	In–phase differential Tx baseband input, negative
20	Q_Tx IN	Quadrature differential Tx baseband input, positive
21	Q_Tx INX	Quadrature differential Tx baseband input, negative
22	V_{CC}_DIG	Supply for digital circuits
23	Tx_ON	One of the Three digital CMOS logic control inputs to the mode control section
24	GNDDIG	Digital ground
25	CLK INX	Differential reference input for synthesizer, negative
26	CLK IN	Differential reference input for synthesizer, positive
28	LO_IN	Differential LO input,positive
29	LO INX	Differential LO input, negative
30	LOCK	Test control output and synthesizer lock indicator
31	STROBE	Serial bus strobe input
32	CLOCK	Serial bus clock input
33	DATA	Serial bus data input
34	V_{CC}CP	Supply for charge pump circuits
35	CP	Charge pump output
36	GNDCP	Ground for charge pump circuits
37	I_{REF}	Charge pump reference current
38	V_{REF}2.5	Reference voltage of 2.5V available for external use
39	V_{CC}TxRx	Supply pin used by Tx circuits
40,41	GNDTxRx	Ground pins used by Tx circuits
42	TxIFOUTX	Differential transmitter IF output (open collector), positive
43	TxIFOUT	Differential transmitter IF output (open collector), negative
45	RxIF INX	Differential receiver IF input, negative
46	RxIF IN	Differential receiver IF input, positive

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{CCXX}+0.3	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXXX}	Supply voltages:	2.7 to 3.6	V
V_{CC}CP	Charge pump supply voltage	2.7 to 3.6	V
T_A	Operating ambient temperature range	-40 to +85	°C

NOTES:
1. There are no ESD protection diodes between pins 42, 43 and V_{CC} to allow higher AC peak voltage. The ESD protection level has thus been reduced. Proper ESD handling precautions should be followed.

MODE CONTROL

NO:	PLL_ON	RX_ON	TX_ON	STATE DESCRIPTION	MODE	2.5V REF
1	0	X	X	SLEEP mode	SLEEP	Off
2	1	0	1	Synthesizer ON, Rx STDBY, Tx OFF	WAIT	Off
3	1	1	1	Synthesizer ON, Rx STDBY, Tx ON	TRANSMIT	On
4	1	1	0	Synthesizer ON, Rx ON, Tx OFF	RECEIVE	Off
5	1	0	0	Synthesizer ON, Rx OFF, Tx ON	TRANSMIT	Off

'0' – LOGIC LOW
'1' – LOGIC HIGH
'X' – DON'T CARE

1. Sleep mode (PLL OFF, Rx OFF, Tx OFF)

In this mode everything is switched off except the 3–wire digital bus. As long as the digital supply is still on, the programmed values are active and the 3–wire bus will continue to be programmable.

2. Wait Mode (Tx Off, Rx Standby)

PLL is on. Receiver is in the reduced current standby mode and the transmitter is completely switched off. This mode maybe useful if the PLL is to be kept on and is waiting for a quick turn–on to either transmit or receive modes, especially when Rx outputs are AC coupled.

3. Transmit mode (Rx standby)

The PLL and transmitter are on. The receive section is in a reduced current mode wherein most of the Rx circuitry is powered down except for the bias and baseband circuits needed to hold the baseband output voltages in the active state. This mode is useful if the Rx baseband outputs are AC coupled via a large capacitor and the application demands quick turn–on for the Rx, from Tx.

4. Receive Mode (Tx Off)

The Transmitter is completely shut–off. The PLL and receiver sections are operating.

5. Transmit Mode (Rx OFF)

PLL and Transmit sections are on. However, the Receiver is completely shut–down. This mode is useful if the Rx baseband outputs are DC coupled to the external world.

RX VGA CONTROL TABLE

GC5	GC4	GC3	GC2	GC1	GC0	DECIMAL NUMBER	REDUCTION FROM Gmax
0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	–2
0	0	0	0	1	0	2	–4
0	0	0	0	1	1	3	–6
0	0	0	1	0	0	4	–8
0	0	0	1	0	1	5	–10
0	0	0	1	1	0	6	–12
0	0	0	1	1	1	7	–14
0	0	1	0	0	0	8	–16
0	0	1	0	0	1	9	–18
0	0	1	0	1	0	10	–20
0	0	1	0	1	1	11	–22
0	0	1	1	0	0	12	–24
0	0	1	1	0	1	13	–26
0	0	1	1	1	0	14	–28
0	0	1	1	1	1	15	–30
0	1	0	1	1	1	23	–32
0	1	1	0	0	0	24	–34
0	1	1	0	0	1	25	–36
0	1	1	0	1	0	26	–38
0	1	1	0	1	1	27	–40
0	1	1	1	0	0	28	–42
0	1	1	1	0	1	29	–44
0	1	1	1	1	0	30	–46
0	1	1	1	1	1	31	–48
1	1	0	1	0	0	52	–50
1	1	0	1	0	1	53	–52
1	1	0	1	1	0	54	–54
1	1	0	1	1	1	55	–56
1	1	1	0	0	0	56	–58
1	1	1	0	0	1	57	–60
1	1	1	0	1	0	58	–62
1	1	1	0	1	1	59	–64
1	1	1	1	0	0	60	–66
1	1	1	1	0	1	61	–68
1	1	1	1	1	0	62	–70

DC ELECTRICAL CHARACTERISTICS

V_{CC}XXX=+3V; V_{EE}XXX = 0V; TA=25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	**TYP**	MAX	
I_{CC-4}	Supply Current, Receive (mode #4)	PLL_ON=Rx_ON=Hi Tx_ON = Low		33.5	41.5	mA
I_{CC-2}	Supply Current, Wait (mode #2)	Wait mode (2) PLL_ON = Hi Tx_ON = Hi Rx_ON = Low		17	23	mA
I_{CC-3}	Supply Current, Transmit (mode #3)	PLL_ON = TX_ON = Hi RX_ON = Hi		26.5	34.5	mA
I_{CC-1}	Supply Current, Sleep mode (mode #1)	PLL_ON = Low RX_ON = DC TX_ON = DC		0.012	0.1	mA
I_{CC-5}	Supply current transmit (mode 5)	PLL_ON = Hi T_X_ON = RX_ON = Low		22	28.5	mA
V_{REF}_2.5	Reference voltage (mode 3, enabled)	Load = 1.5mA		2.5		V
Z_{OUT}_V_{REF}	Output impedance of reference voltage	ΔI = 1.4 to 1.6mA		15		Ω
CMOS LOGIC INPUTS (DATA, CLOCK, STROBE)						
V_{IH}	Input logic 1 level		2.0		V_{CCD}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	μA
C_I	Input logic capacitance				4	pF
CMOS Logic output (LOCK)						
V_{OH}	Output logic 1 level	I_O = –2mA	V_{CCD}–0.4			V
V_{OL}	Output logic 0 level	I_O = 2mA			0.4	V
CMOS Logic Inputs (PLL_ON, RX_ON, TX_ON)						
V_{IH}	Input logic 1 level		2.0		V_{CCTXRX}	V
V_{IL}	Input logic 0 level		0		0.8	V
I_I	Input logic current				1	μA

AC ELECTRICAL CHARACTERISTICS IF TRANSMIT MODULATOR

(Mode #3, Tx ON Rx Standby) V_{CC}XXX = +3V; GNDXXX = 0V; LO_in = 100 mV peak at 704 MHz, CLKin = 100mV peak at 22 MHz, T_{amb} = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	TYP	MAX	
BW[4,5]	Input modulation bandwidth	500 ohms source impedance	22			MHz
V_{IN}	Input signal amplitude, Differential[1]	Voltage common mode = 1 to 2V		1		Vpp
THD_3	Third harmonic distortion[5]	Input signal amplitude = 1 V_{PP}, 8 MHz, V_{CM} = 1.5		–55	–45	dBc
R_{INTx}	Input resistance	Between pins I_T_XIN, I_T_XINX Q_T_XIN, Q_T_XINX		98		kΩ
C_{INTx}[4]	Input Capacitance	Between pins I_T_XIN, I_T_XINX Q_T_XIN, Q_T_XINX			2	pF
	Minimum Tx output DC voltage	V_{IN} = IV_{PP} V_{CM}I = V_{CM}Q = V_{CC}/2		V_{CC}–0.3		V
IO DC	Mean output DC current	At $T_X IF_{OUT}$ and $T_X IF_{OUTX}$		2	2.75	mA
	Output current DC offset[4]	Mismatch at $T_X IF_{OUT}$ and $T_X IF_{OUTX}$			40	µA
	Output current available[2]	At $T_X IF_{OUT}$ and $T_X IF_{OUTX}$		0.475		mA rms
	Output differential voltage[1,2]	400 Ω tuned load[2]		190		mV rms
CS	Carrier suppression[1,3]	Differential output	30	36		dBc
SBS	SB Suppression [1,3]	f_{OUT} = 352 MHz	35	47		dBc
	Noise floor	offset = 10 MHz		156		dBc/Hz
ΔG[4]	Gain stability[6]			0.5	2.0	dB
t_{ON}[4]	Turn–on time	T_X_ON, R_X_ON transition to transmit signal at 90% level		4		µs
T_{OFF}[4]	Turn–off time	T_X_ON, R_X_ON transition to transmit signal at 10% level		4		µs

NOTES:

1. Tx inputs are differential sine wave, 0.5 V peak, with quadrature relationship between I and Q Tx input. The output spectrum will be SSB. The tone is at a frequency of 1 MHz.
2. The output current in each arm is the same but 180 degrees out of phase with each other. Also the tuned load of 400 ohms differential, is assumed. The power delivered to 400 ohms will be –10.4 dBm (typ.). The output current measurement is indirect based on output power measurement according to P = 10 log I^2rms (400Ω)/IMV. See typical performance characteristic curve.
3. This is measured with respect to the SSB output.
4. Guaranteed by design and or characterization but not final tested.
5. The input bandwidth may be verified by measuring the output THD and signal level using a DSB spectrum where I = Q.
6. Measured over temperature and supply.

AC ELECTRICAL CHARACTERISTICS IF RECEIVER DEMODULATOR

(Mode #4, Rx_ON, Tx_OFF) V_{CC}XXX = +3V = GNDXXX = 0V; LO IN = 100 mV_{peak} at 704 MHz, CLKIN = 100mV_{peak}, at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	TYP	MAX	
RInRx	Differential input impedance	f_{IN} = 352 MHz		6.6K||0.7		kΩ||pF
VG	Voltage gain	AGC at maximum gain	81	88		dB
NF	Input noise figure[1]	VGA at maximum gain		7.5		dB
	AGC range		67	70		dB
	AGC step size			2		dB
	AGC differential error				2	dB
	AGC settling time	any AGC step			200	nS
	Channel matching gain phase			0.1 0.25		dB deg
	Output DC offset between IRx Out and QRx Out	Maximum Gain, Output at 1 MHz		6		mV
OVS	Output voltage swing	AGC G_{MIN}, into load[2]	0.9	1.15		Vp–p
		AGC Gain, except G_{MIN}	1.0	1.4		
	Output common mode voltage			1.9		V
	Output impedance			7		Ω
THD[3]	Total Harmonic Distortion	Max. Gain, rated output at 1 MHz		3		%
BW[5]	Rx Bandwidth		7	8.5	10	MHz
t_{ON}[4]	Turn–on time	R_X_ON, T_X_ON transition to baseband signal out			2	µs
t_{OFF}[4]	Turn–off time	R_X_ON, T_X_ON transition to no baseband signal out			2	µs

NOTES:

1. The Receive input is to be differential (using a balun or a differential source such as a differential SAW filter) and matched to external generator's impedance (ex: 50 ohms). The balun may or may not provide any impedance transformation depending on availability. An external L–C matching circuit can provide the rest of the impedance transformation and absorb the input capacitance of the receiver input. Such a differential input scheme is mandatory to avoid pickup, and keep the noise figure low. A shunt resistor across the input (value TBD) will be used to set the input impedance as a compromise between the matching ease in production versus the noise figure of the receiver. The system board layout has to keep the isolation between the receive inputs and the LO signal as high as possible. Otherwise the LO leakage will overload the receiver.
2. The load is 1000 ohms in parallel with 15pF of capacitor.
3. THD is total harmonic distortion. We measure harmonics 2, 3, 4.
4. Guaranteed by design.
5. 3dB bandwidth relative to a passband measurement taken at 1MHz.

AC ELECTRICAL CHARACTERISTICS IF SYNTHESIZER

V_{CC}XXX = RX_ON = TX_ON = PLL_ON = +3V, V_{EE}XXX = 0V; LO_IN = 100 mV_{peak} at 704 MHz, CLKIN = 100mV_{peak} at 22 MHz, Ta = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MIN	TYP	MAX.	
f_{LO}	Local oscillator input frequency range[3]		140		800	MHz
Z_{LOIN}	Differential input impedance	Between LO_IN and LO_INX		276||0.6		Ω||pF
V_{LOIN}	LO input sensitivity[4]	Single ended Referred to 50Ω	50		350	mVpk
	Programmable divider: division range step size		64	 1	511	
f_{CLK}	Reference clock maximum frequency[3]		1	44		MHz
Z_{CLKIN}	Differential input impedance	Between Clk_{IN} and Clk_{INX}		10|| 1.0		kΩ pF
	CLK input sensitivity[4]	Referred to 50Ω	50	200	400	mVpk
f_{CMIN}	Phase detector minimum comparison frequency			1		MHz
f_{CMAX}	Phase detector maximum comparison freq	Ref Divider = 44		2.5		MHz
I_{REF}	Charge pump reference current	R_{EXT} = 50KΩ		31.25		µA
$\|I_{CP}\|$	Charge pump output current: C0...C2 = 000 C0...C2 = 111 step size	I_{REF} = 31.25 µA V_{CP} = V_{CC}CP/2	0.160 0.320 0.023	0.200 0.400 0.029	0.240 0.480 0.035	mA mA mA
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[1]	I_{REF} = 31.25 µA		1.3	±8	%
ΔI_{CP_M}	Output current matching[2]	I_{REF} = 31.25 µA V_{CP} = V_{CC}CP/2			±12	%
	Output leakage current			0.2	±15	nA
	Output current tolerance with temperature with output voltage			 ±1 ±5		%
Serial Interface[3]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set–up time; DATA to clock, CLOCK to STROBE		30			ns
t_H	Hold time: CLOCK to DATA		30			ns
t_W	Pulse width: CLOCK		30			ns
	Pulse width: STROBE		30			ns

NOTES:

1. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{I(I_2 + 1_1)}$; WITH V_1 = 0.7V, V_2 = V_{CC}CP – 0.8V (see Figure 3).
2. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on
3. Guaranteed by design.
4. Maximum level guaranteed by design.

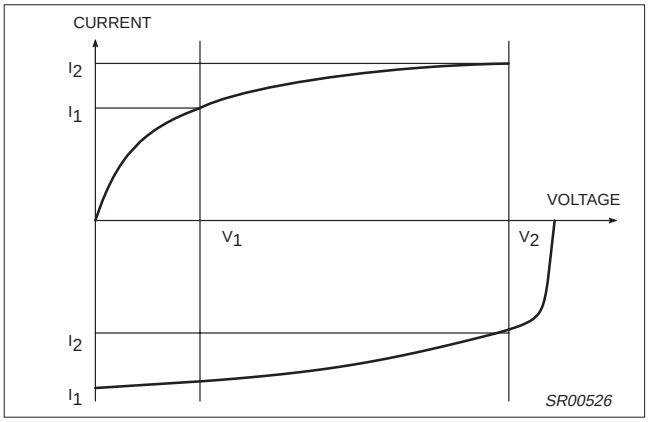


Figure 3. Relative Output Current Variation

APPLICATION DESCRIPTION

General

The 1630 performs the IF modulator and demodulator functionality for high–speed wireless data transceivers. The design is optimized for IEEE 802.11 wireless LAN using 11 chips/symbol Direct Sequence Spread Spectrum.

Transmitter

The IF quadrature transmitter baseband modulator input is driven differentially by the D/A converters in the DSP chip. The baseband signals are DC coupled for fast turn–on and turn–off and for constant carrier testing. The typical common–mode input voltage is VCC/2.
The open collector outputs of the mixers are biased by two inductors, which are part of an LC tank. The LC tank matches the output impedance of the mixers to the input impedance of the upconverter chip (or any filter in between) and suppresses IF harmonics.

An optional 2.5V reference is available during mode (3) and (5), the transmit mode with Rx in standby. This reference can be enabled or disabled via the 3 wire bus (in this mode). This voltage is provided for use by an external current DAC if needed.

Receiver

The receiver part of the SA1630 consists of an IF Variable gain amplifier, a quadrature demodulator and a pair of baseband amplifiers. The IF amplifier has its gain controlled by the DSP chip. This ensures linear operation of the receiver chain over a wide dynamic range of input signals. Linear operation is essential for resolving echo's due to multipath reception.

The digital controlled AGC is meant for fast level training for the receiver.

The high gain receiver, which is distributed between the IF and baseband part facilitates interfacing with the RF front–end chip, which normally have moderate gains (up to 20 dB), and SAW IF filters, which mostly have considerable loss (up to 8 dB) without external amplifiers.

The baseband amplifiers have a high drive capability (1 Vpp into 1kΩ, 15 pF for VCC = 3V) that facilitates direct interfacing to the A/D converter without active external elements.

The baseband amplifiers can interface directly to the Track/Hold switch/capacitor combination with capacitance values up to 15 pF. When sampled at 22MHz the output can settle to within 1/4 LSB when swinging 1V p–p.

The chip has a unique mode in which the Rx is on standby while the Tx is ON. In this mode the Rx Baseband circuits are idling at reduced currents and all Rx I/O outputs retain their DC bias unchanged from their values when the Rx was fully ON. This mode is very essential if ac coupling through a large capacitor, such as, 10nF is used. From this mode the chip can quickly be switched to the Rx ON mode (Tx OFF) without worrying about charging/discharging the large AC coupling capacitor.

The VGA can be programmed in 2 ways: 1) Directly programming external control pins. 2) programming over the serial 3–wire bus. The former method can switch gain in less than 200 ns.

The Rx baseband section also incorporates simple low pass active filters of the Sallen key type. The Rx bandwidth is mainly set by these filters. The function of these filters is twofold: 1) attenuate high frequency signals from the Rx mixers. 2) act as anti–aliasing filters for any A to D converters following this chip.

IF synthesizer

The SA1630 has an integrated synthesizer that uses an external VCO operating on twice the IF frequency. It is internally divided by 2 for obtaining quadrature signals. The divided VCO signal is not externally available. This minimizes the LO feedthrough to the IF input port and hence minimizes output dc glitches when the IF gain is switched.

The PLL reference clock is derived from the 22 MHz DSP clock. The available divider ratios facilitate both 1 and 2 MHz phase comparison frequency from a 22 MHz and an optional 44 MHz clock respectively. In essence the reference divider will have programmable dividers ratios of 8, 11, 22 and 44.

The VCO shall be fed from a stabilized supply. Such a stabilized supply is necessary in order to prevent oscillator jitters due to Rx/Tx switching. The effect of oscillator jitters is further minimized when using a high PLL loop bandwidth, which on its turn requires a high phase comparison frequency (1 MHz, preferably 2 MHz).

If the IF Synthesizer is not used, the CLK_{IN} pins should be terminated to ac ground.

Serial Programming Input

The serial input is a 3–wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status– and DC–offset register, mode select and test register. The programming data is structured into two 21–bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 3 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. The logic level at the

STROBE pin should be low during power up to guarantee a proper reset. These default states are shown in Table 2.

Reference Divider

The reference divider can be programmed to four different division ratios (:8, :11, :22, :44), see registers r0, r1; default setting: divide by 22.

Main Divider

The external VCO signal, applied to the LO_{IN} and $LO_{IN}X$ inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 352.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure 5. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump acts to increase the VCO frequency; a sink current acts to decrease the VCO frequency.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and $V_{EE}CP$. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and $V_{EE}CP$. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.6V}{31.2\mu A} \quad (44.87K \text{ for } 3V)$$

The current can be set to zero by connecting the pin I_{REF} to $V_{CC}CP$.

Charge Pumps

The charge pumps at pin CP are driven by the phase detector and the current value is determined by the binary value of the charge pumps register CN = c2, c1, c0, default .4mA. The active charge pump current is typically:

$$|I_{CP}| = (c0 + 2c1 + 4c2) \cdot 29\mu A + 200\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, $CLK_{IN}X$.

Test Modes (Synthesizer, Transmit Mixer)

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path. Setting x0,1 = 11 disables both transmit path mixers. This mode can be used to prevent the transmitter from producing an IF output signal even if the transmit part is powered on. This can be used to simplify the control timing while commanding the transmit and receive simultaneously without the transmit part causing interference.

Table 1. Test Modes

x0	x1	Synthesizer Signal at LOCK Pin	Transmit Mixer	
			Q-mixer	I-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	$LO_{IN} \div 2$ * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Table 2. Definition of SA1630 Serial Registers

First data word: (shown with default values)																				
Address SA1630				**Sub Adr**	**N-Divider**									**Reference Divider**		**Charge-Pump**			**Test**	
MSB																				**LSB**
a0	**a1**	**a2**	**a3**	**sa**	**n0**	**n1**	**n2**	**n3**	**n4**	**n5**	**n6**	**n7**	**n8**	**r0**	**r1**	**c0**	**c1**	**c2**	**x0**	**x1**
1	1	1	0	0	1	0	1	1	0	0	0	0	0	1	0	1	1	1	0	0
Address:					4 bits, a0...a3, fixed to 1110															
Sub:Address:					1 bit, sa, fixed to 0 for first data word															
N-Divider:					9 bits, n0...n8, values 64 (00100 0000) to 511 (11111 1111) allowed for IF choice, default 352 (assuming LO input frequency is 704 MHz).															
Reference Divider Register:					2 bits, r0...r1, 00 = /8, 01 = 11, 10 = /22, 11 = /44. Default: 10															
Charge-Pump Register:					3 bits, c0...c2, Binary setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default is maximum charge pump current (111)															
Test Register:					2 bits, x0...x1, default 00, see functional description for details															
Second data word: (shown with default values)																				
Address SA1630				**Sub Adr**	**LLL Mode Control**		**I Offset Register**			**Q Offset Register**			**VGA Gain Control**						**Misc Control bits**	
MSB																			**LSB**	
a0	**a1**	**a2**	**a3**	**sa**	**s0**	**s1**	**i0**	**i1**	**i2**	**q0**	**q1**	**q2**	**b0**	**b1**	**b2**	**b3**	**b4**	**b5**	**bc**	**vc**
1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
Address:					4 bits, a0...a3, fixed to 1110															
Sub:Address:					1 bit, sa, fixed to 1 for second data word															
LLL Mode control:					2 bits, s0, s1 Not used, always set to 0, 0															
I Offset Register:					3 bits, i0...i2 .10 Not used, always set to 0, 0, 0															
Q Offset Register:					3 bits, q0...q2. q0. Currently not being used, always set to 0, 0, 0															
VGA Gain Control					6 bits, b0...b5. 000 000 corresponds to maximum gain and 111 111 to minimum gain in 2 dB increments. Check control table contained elsewhere in this document.															
VGA Control Enable					1 bit, bc. When bc=0 the VGA is controlled by external pins. When bc=1 then bits b0...b5 control the VGA. Default bc=0, control by external pins															
Regulator Disable					1 bit, Vc. When Vc=0 the 2.5V reference output is completely powered down. When Vc=1 the reference voltage is enabled (provided Tx_ON=HIGH). Default: Vc = 1, enable the 2.5 reference.															

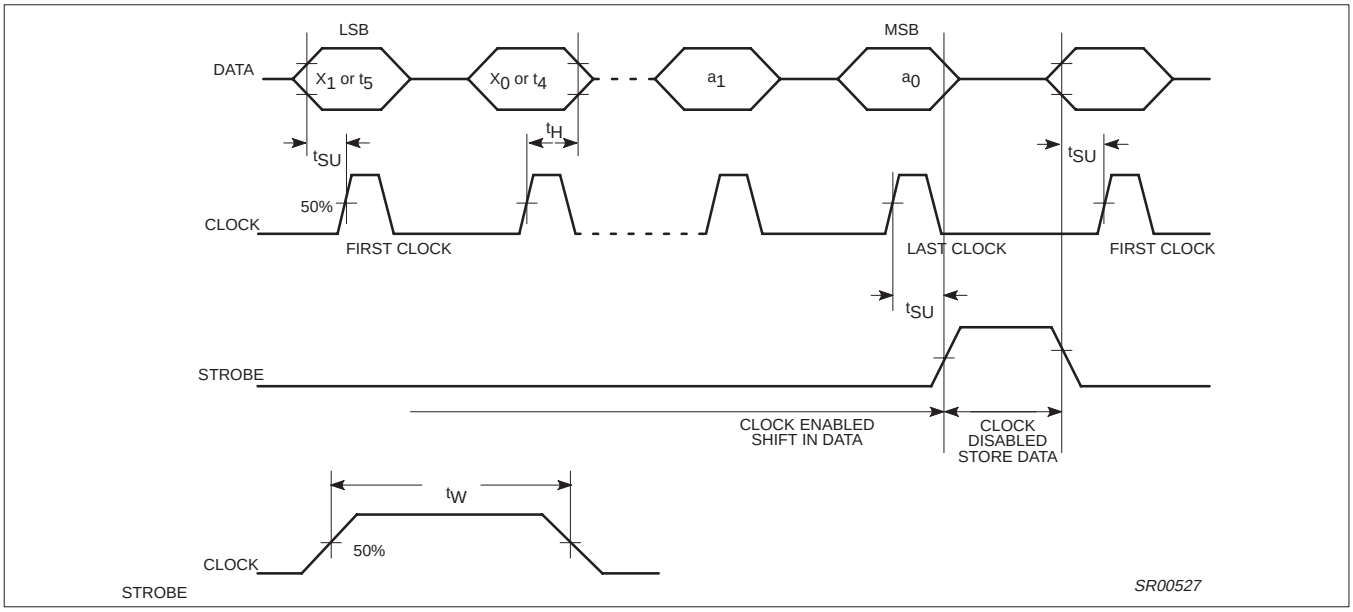


Figure 4. Serial Input Timing Sequence

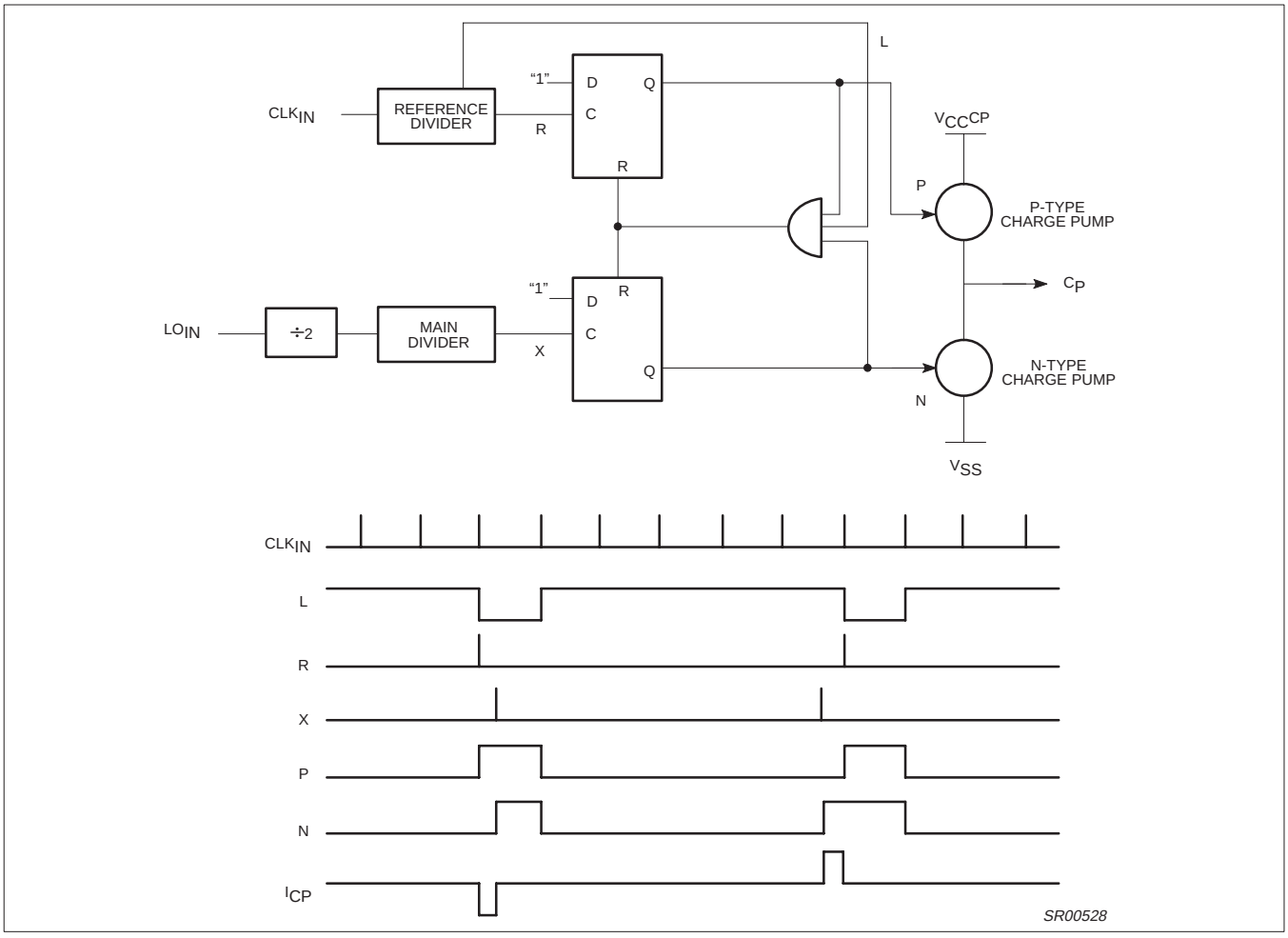


Figure 5. Phase Detector Structure with Timing

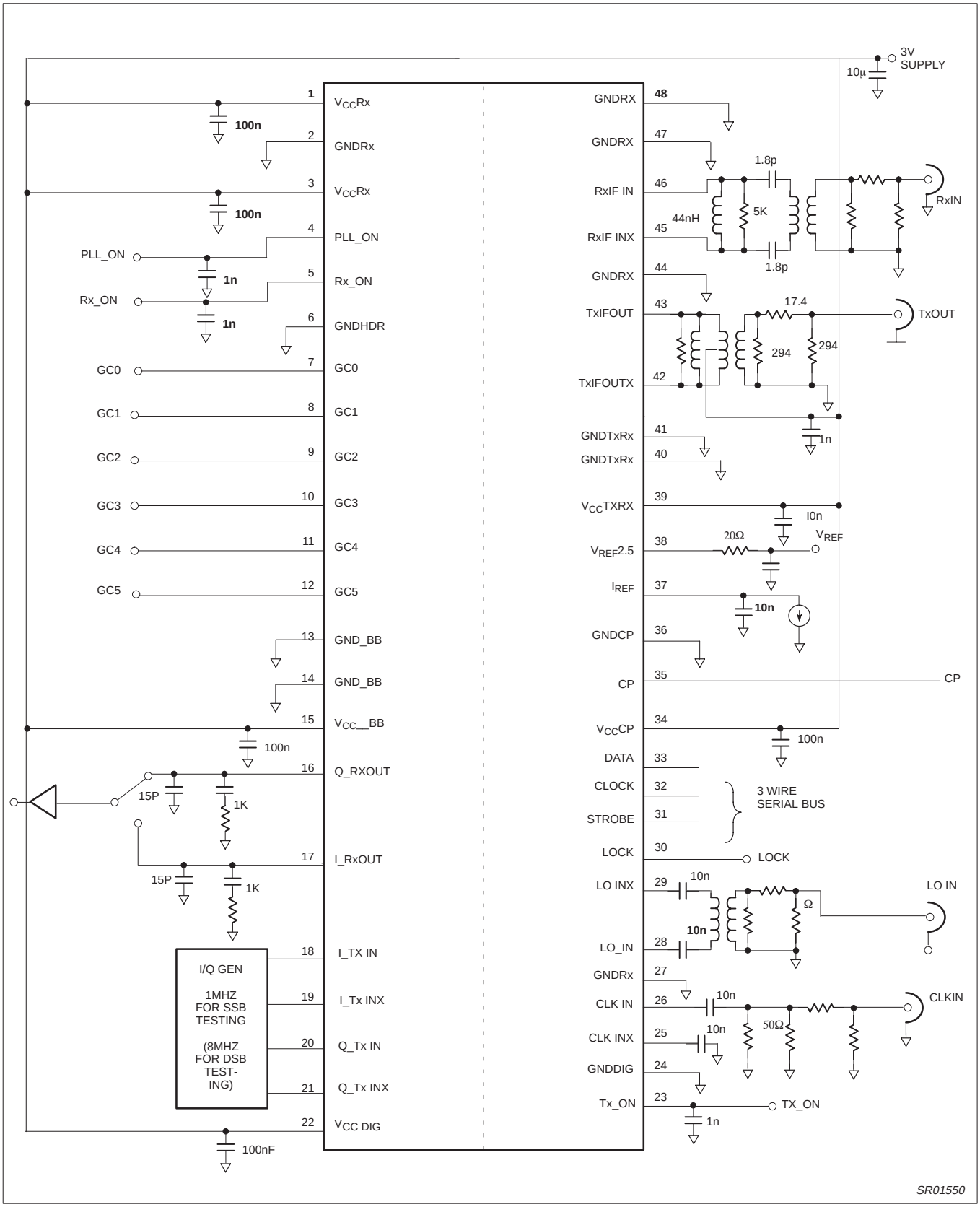


Figure 6. Typical SA1630 Test Circuit

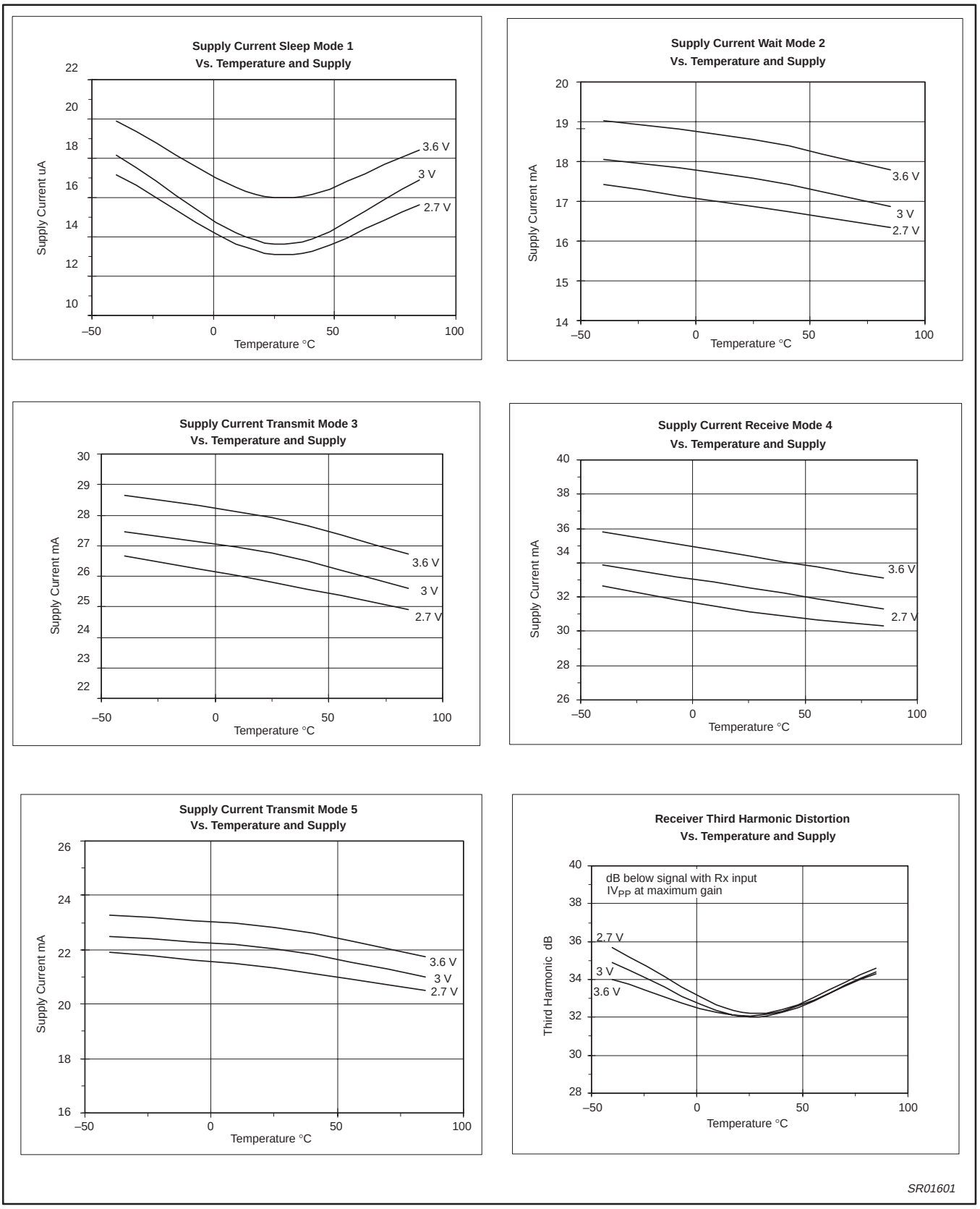

Supply Current Sleep Mode 1
Vs. Temperature and Supply
Supply Current uA
Temperature °C
3.6 V
3 V
2.7 V
Supply Current Wait Mode 2
Vs. Temperature and Supply
Supply Current mA
Temperature °C
3.6 V
3 V
2.7 V
Supply Current Transmit Mode 3
Vs. Temperature and Supply
Supply Current mA
Temperature °C
3.6 V
3 V
2.7 V
Supply Current Receive Mode 4
Vs. Temperature and Supply
Supply Current mA
Temperature °C
3.6 V
2.7 V
Supply Current Transmit Mode 5
Vs. Temperature and Supply
Supply Current mA
Temperature °C
3.6 V
3 V
2.7 V
Receiver Third Harmonic Distortion
Vs. Temperature and Supply
dB below signal with Rx input
IVPP at maximum gain
Third Harmonic dB
Temperature °C
2.7 V
3 V
3.6 V
SR01601

Figure 7.

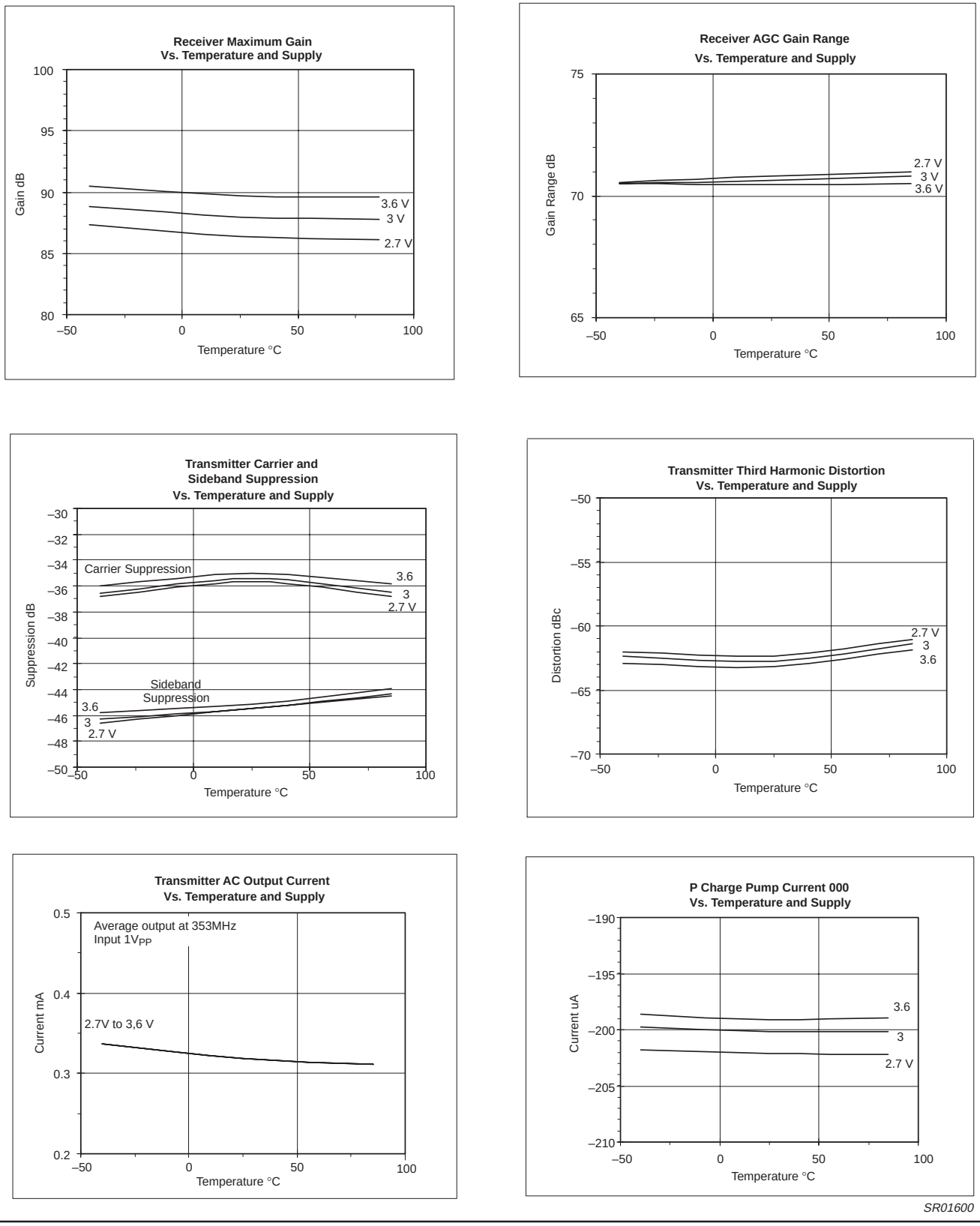
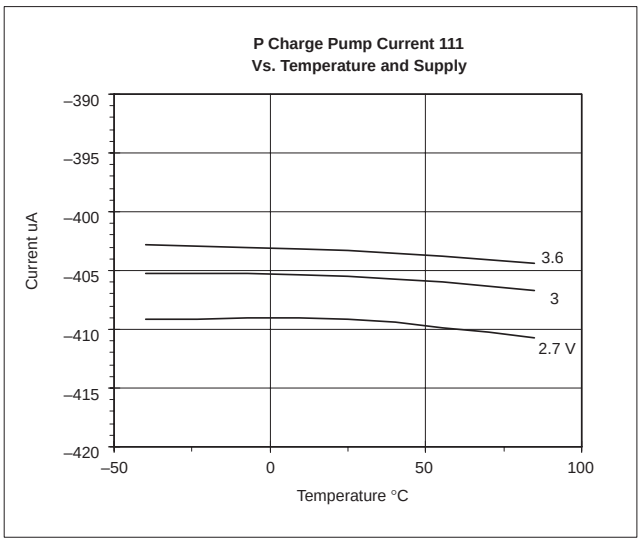
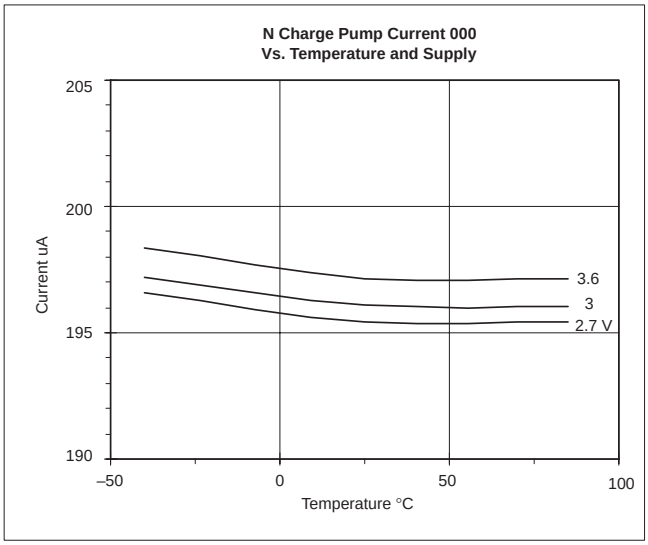
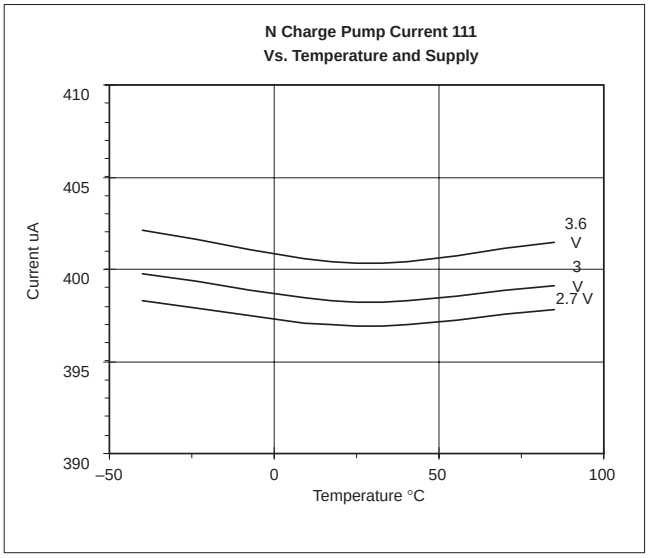
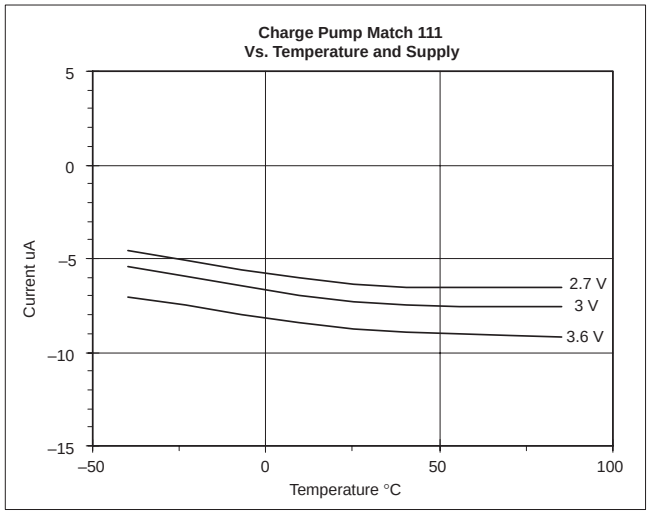

Receiver Maximum Gain
Vs. Temperature and Supply
Gain dB
100
95
90
85
80
–50
0
50
100
Temperature °C
3.6 V
3 V
2.7 V
Receiver AGC Gain Range
Vs. Temperature and Supply
Gain Range dB
75
70
65
–50
0
50
100
Temperature °C
2.7 V
3 V
3.6 V
Transmitter Carrier and
Sideband Suppression
Vs. Temperature and Supply
Suppression dB
–30
–32
–34
–36
–38
–40
–42
–44
–46
–48
–50
–50
0
50
100
Temperature °C
Carrier Suppression
3.6
3
2.7 V
Sideband
Suppression
3.6
3
2.7 V
Transmitter Third Harmonic Distortion
Vs. Temperature and Supply
Distortion dBc
–50
–55
–60
–65
–70
–50
0
50
100
Temperature °C
2.7 V
3
3.6
Transmitter AC Output Current
Vs. Temperature and Supply
Current mA
0.5
0.4
0.3
0.2
–50
0
50
100
Temperature °C
Average output at 353MHz
Input 1VPP
2.7V to 3,6 V
P Charge Pump Current 000
Vs. Temperature and Supply
Current uA
–190
–195
–200
–205
–210
–50
0
50
100
Temperature °C
3.6
3
2.7 V
SR01600

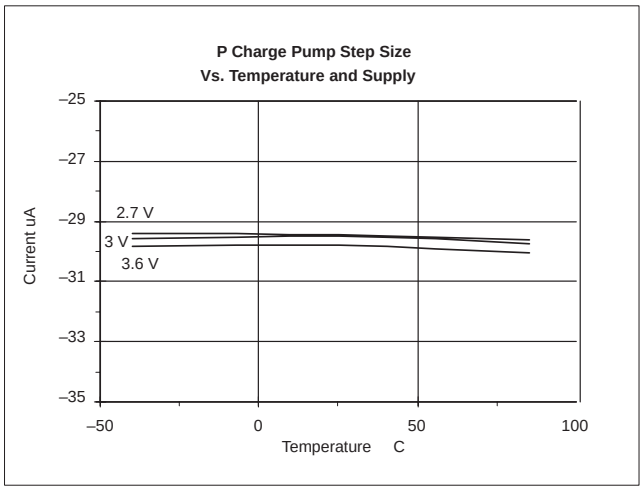
Figure 8.

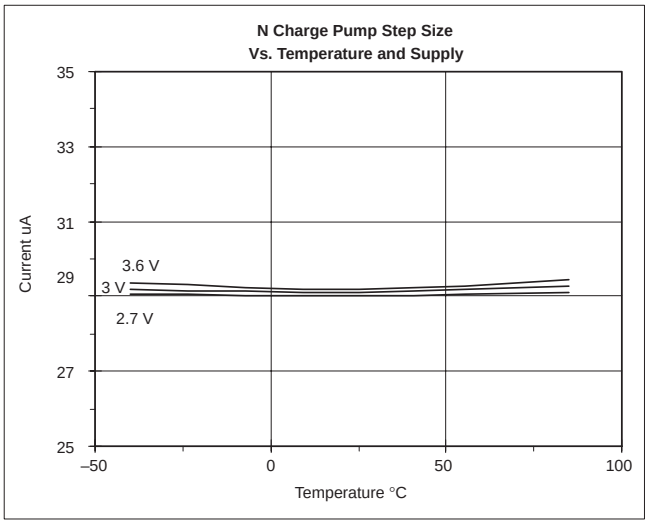












SR01599

Figure 9.

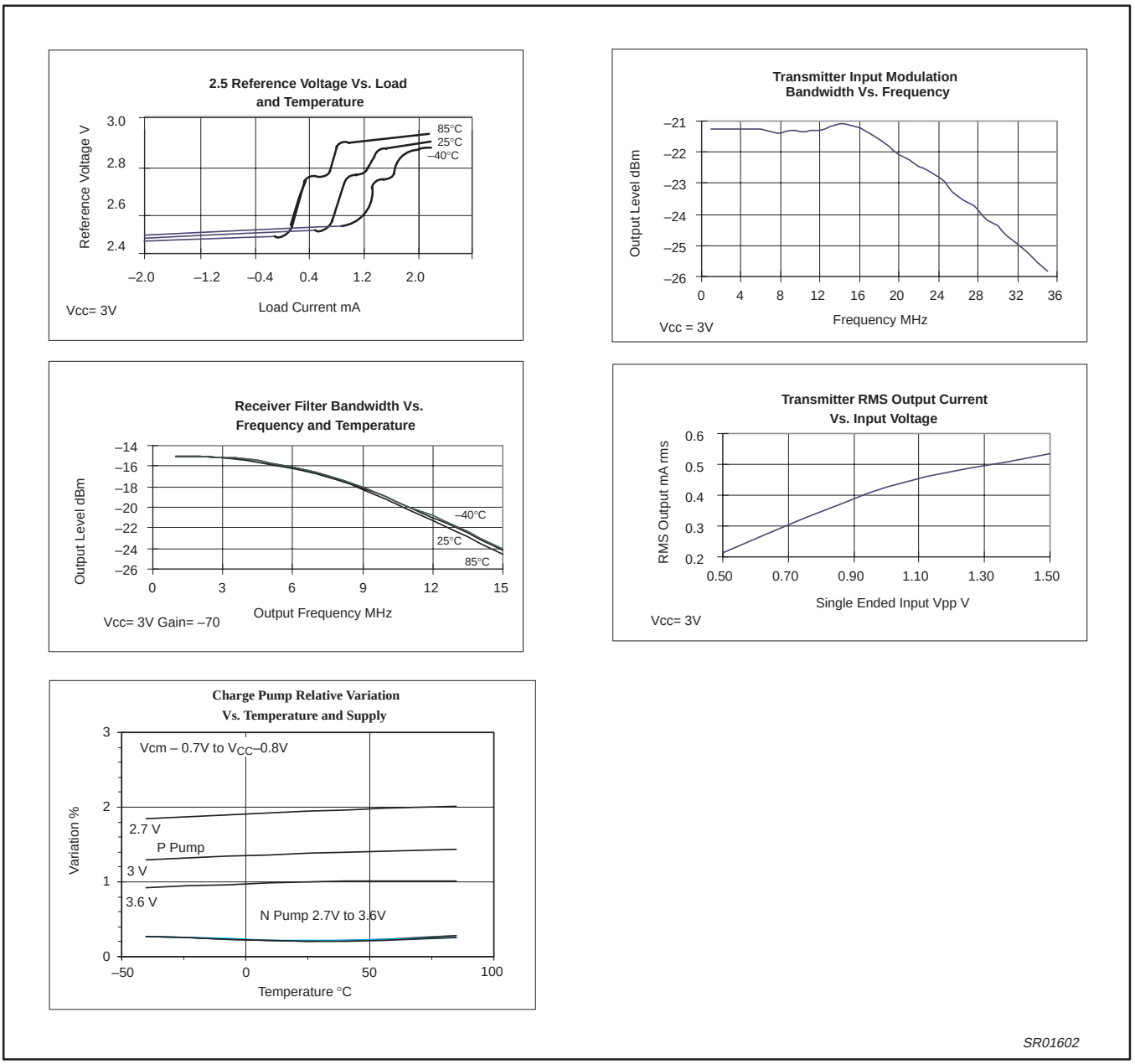
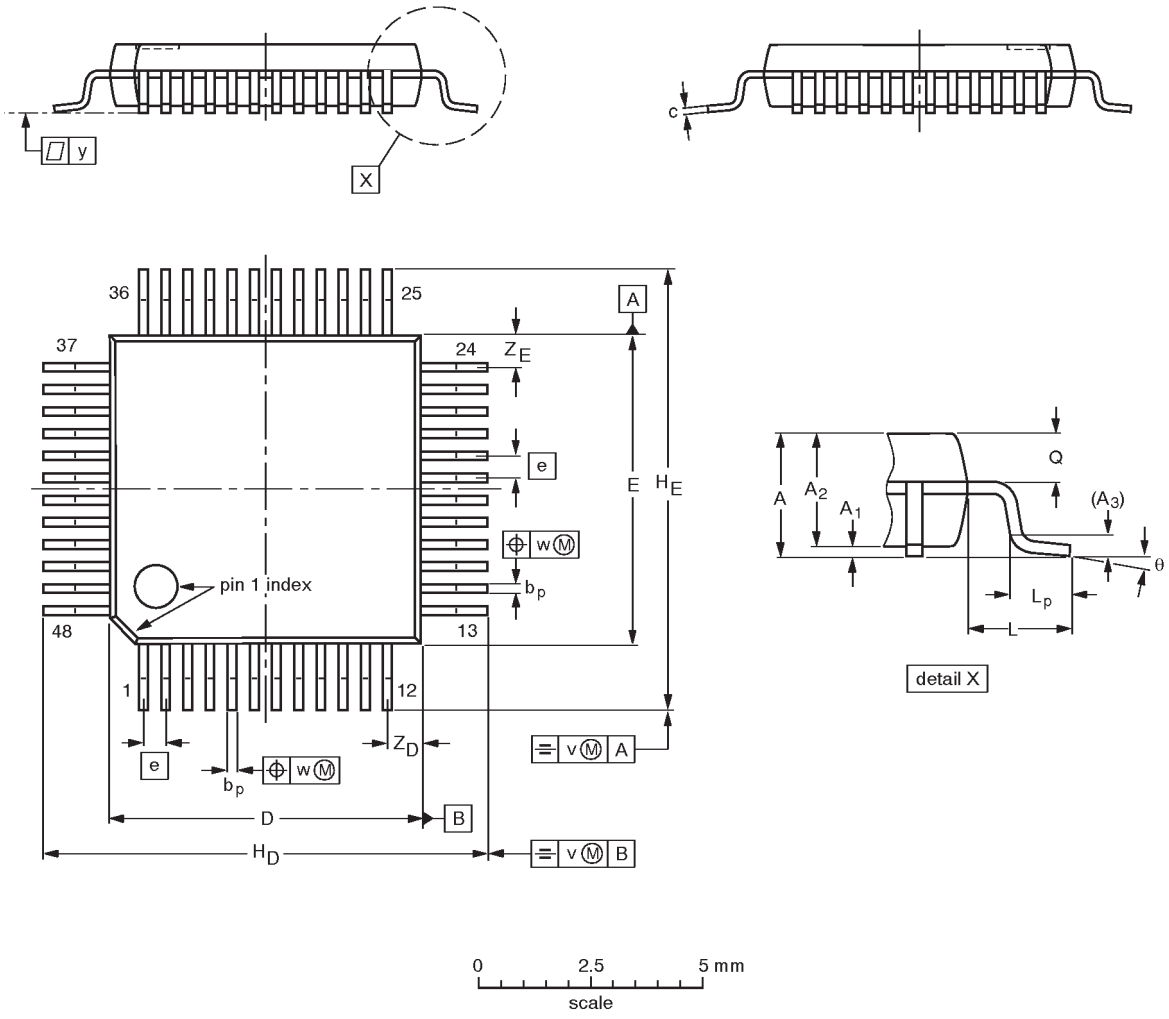

2.5 Reference Voltage Vs. Load and Temperature
Reference Voltage V
3.0
2.8
2.6
2.4
85°C
25°C
–40°C
–2.0
–1.2
–0.4
0.4
1.2
2.0
Load Current mA
Vcc= 3V
Transmitter Input Modulation Bandwidth Vs. Frequency
Output Level dBm
–21
–22
–23
–24
–25
–26
0
4
8
12
16
20
24
28
32
36
Frequency MHz
Vcc = 3V
Receiver Filter Bandwidth Vs. Frequency and Temperature
Output Level dBm
–14
–16
–18
–20
–22
–24
–26
–40°C
25°C
85°C
0
3
6
9
12
15
Output Frequency MHz
Vcc= 3V Gain= –70
Transmitter RMS Output Current Vs. Input Voltage
RMS Output mA rms
0.6
0.5
0.4
0.3
0.2
0.50
0.70
0.90
1.10
1.30
1.50
Single Ended Input Vpp V
Vcc= 3V
Charge Pump Relative Variation Vs. Temperature and Supply
Variation %
3
2
1
0
Vcm – 0.7V to VCC–0.8V
2.7 V
P Pump
3 V
3.6 V
N Pump 2.7V to 3.6V
–50
0
50
100
Temperature °C
SR01602

Figure 10.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

NOTES

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Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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